



Features

- For use in WiMAX systems. Fully compliant with the WiMAX standard IEEE std 802.16-2004
- Generic memory interface for easy ASIC integration
- Simple handshake protocol for reliable interfacing
- Fully synchronous design
- Full WiMAX compliant hardware interleaver. No external calculation required.
- Interleaver frame size selectable on a frame-by-frame basis
- All defined block sizes supported
- Comprehensive verification plan provided
- All defined rates (1/2, 2/3, 3/4, 5/6, 7/8) supported

General Description

The SAL50101D consists of verilog IP for decoding the 8-state turbo code defined by the WiMAX standard.

The decoder takes in 6-bit values for the unencoded (“systematic”) data and a number of parity values, depending on the code rate. Some of the parity values are the result of encoding the data with a simple convolutional encoder and some are the result of encoding a permutation of the data through an identical simple convolutional encoder. The data are operated on iteratively by the Soft Output Viterbi Algorithm (SOVA) decoder module, first looking at the normal ordered data and parity, then looking at the interleaved sequence and parity. At each step in the process a correction factor is refined and stored as “extrinsic” data for use in the following step.

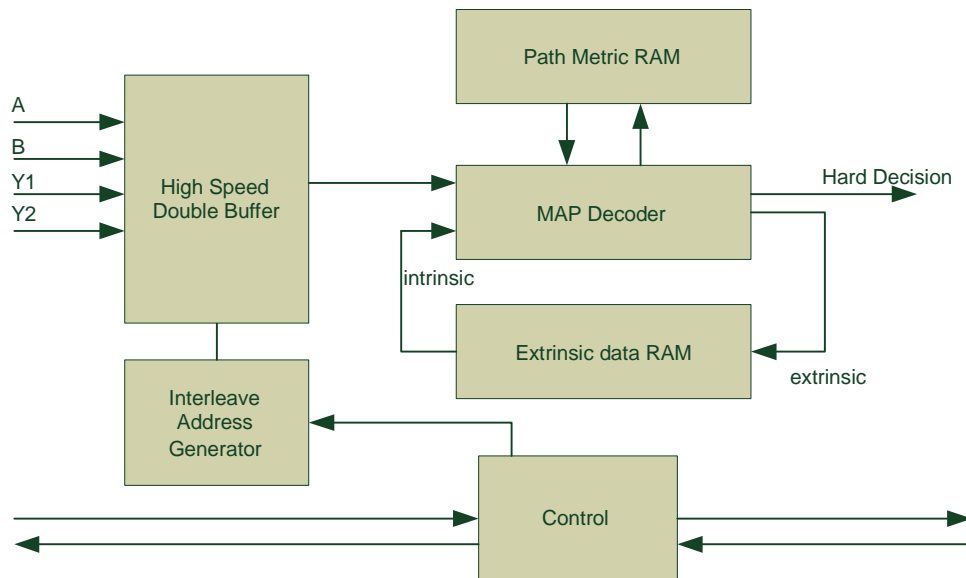


Figure 1: Decoder Block Diagram

Theory of Operation

The SAL50101D is a self-contained, high quality error correction coder designed specifically for use in 802.16 compliant systems. The emphasis for the SAL50101D product is on achieving superior error correction performance at a moderate complexity. The reader is referred to the SAL50100D product for our lower power / performance solution. For the highest bit-rate performance (at the expense of higher complexity) the reader is referred to the SAL50102D product.

The device receives 6-bit 2's-compliment data for unencoded data, parity, and interleaved parity. Data can also be received as signed-magnitude or unsigned binary, based on the *input_mode* signal.

in_mode[1:0]	definition
00	6-bit 2's compliment
01	6-bit signed magnitude
10	6-bit unsigned binary
11	6-bit 2's compliment

Table 1. input_mode

The heart of the decoder is a soft-in / soft-out (SISO) decoder module that performs the SOVA algorithm iteratively.

The Decoder Constant

Because the decoder core operates in the logarithmic domain, the input data need to be converted to a logarithmic (log likelihood ratio) form. This reduces to multiplication of

the input data by a constant based on the estimated signal to noise ratio of the channel.

The value of the decoder constant is calculated using the formula:

$$C = A\sigma^2\sqrt{m/2} \quad (1)$$

Where σ^2 is the normalized noise variance. It has been shown [2] that no noise estimation is better than poor noise estimation, so the input scaling can optionally be disabled.

Max Extrinsic

In addition to input scaling, the extrinsic correction term can be limited to limit the rate at which the decoder converges on a solution.

Num Iterations

The number of decoder iterations can be specified using the *num_its* signal. The default value is 4.5. Optionally the device can be allowed to perform early termination, if the decoder converges on a solution before the specified number of iterations.

Mode Bits

There are a number of mode bits beside the input and output mode bits, and they are shown in the table below.

mode[3:0]	definition, if set
mode[0]	Use decoder_const
mode[1]	Use max_extr
mode[2]	Use num_its, else use 4.5 iterations
mode[3]	Use early termination, if possible

Table 2. mode bits

Allowable information block lengths

The code consists of blocks of k bits or N couples ($k=2N$ bits). For all frame sizes, k is a multiple of 8 (N is a multiple of 4). N is limited to values between 8 and 256. Zero padding should be used for block sizes less than 32 bytes.

Device Operation

Decode operation begins when the ***start_decode*** signal is asserted. In devices with double-buffered input the device will accept a second data block while processing the first.

Signal Descriptions

The module pinout is shown in the figure below, and in table 1. The signals are conveniently organized into functional groups as follows:

Clock and Reset

The design is fully synchronous with a single clock signal. The reset signal is synchronous and needs to be asserted for at least one full clock cycle to reset internal logic.

Control signals

Init, *frame_size*, *d_const*, *max_extr*, and *in_mode* are control signals whose operation is described below.

Data signals

The *din_a*, *din_b*, *din_y1* and *din_y2* are 6-bit input signals representing the systematic data and the parity signals defined in the spec. *Dout* is the serial output decoded data.

The data input to the device are stored internally in FIFO order, the first bit being bit 0 of the data frame. In addition to the data frame, the device expects to see 4 trellis termination or “tail” bit periods as defined in the spec.

The data out of the device are in FIFO order, and therefore don’t require an address to access them. The data can either be read out in serial fashion on bit 0 of *dout*, or in parallel fashion, depending on the value of *out_mode*.

Flow control signals

The “rdy_in_n” signals are active low indicators to the device that data is available on the input or that the external logic is able to accept data.

The “rdyout_n” signals are active low indicators from the device that it is ready to accept data on the input or to shift out data on the output

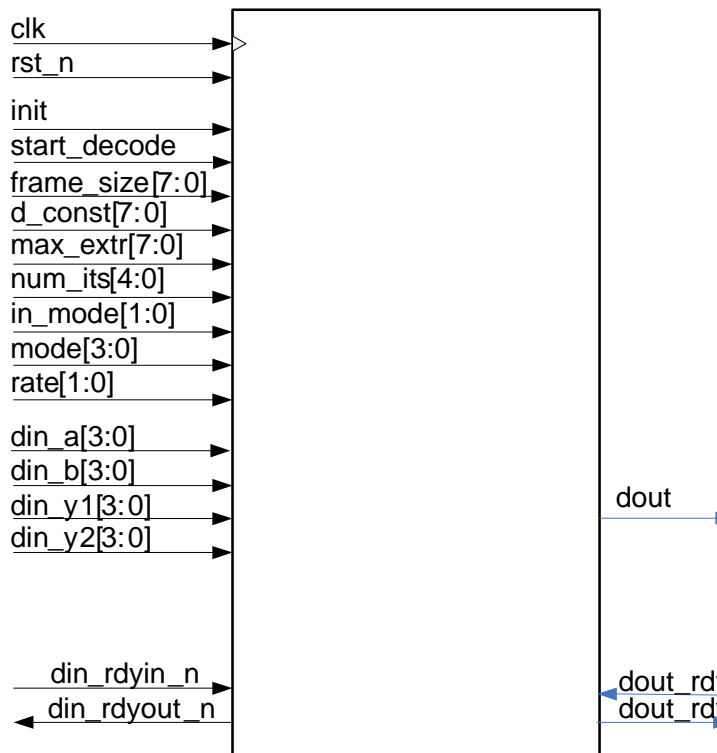


Figure 2: Component Pinout

Pin	Sense	Width	Description
clk	in	1	clock
rst_n	in	1	synchronous reset
din_a	in	6	data (message) in
din_b	in	6	data (message) in
din_y1	in	6	parity data in
din_y2	in	6	parity data in
din_rdyin_n	in	1	indicates serial data in is valid
din_rdyout_n	out	1	indicates module ready to accept data (not all input buffers full)
dout	out	1	decoded data out
dout_rdyin_n	in	1	indicates to the module that it's ok to shift data out
dout_rdyout_n	out	1	indicates that data is available to be shifted out
init	in	1	initializes the interleaver and loads the block size
start_decode	in	1	decoding begins when this signal is asserted
frame_size	in	3	indicates size of current block. Initialized with "init" signal.
num_its	in	5	maximum number of iterations
dec_const	in	8	decoder constant, based on estimated noise (see description above)
max_extr	in	8	maximum allowable extrinsic data (see description above)
in_mode	in	2	input mode: specify the data format of input bits
mode	in	4	various mode bits affecting device operation
rate	in	3	Code rate: 000 = 1/2, 001 = 2/3, 010 = 3/4, 011 = 5/6, 100 = 7/8

Table 3. Pin Definitions

Waveforms

Initialization

The frame size defaults to 1784 bits (the minimum number specified in the WIMAX spec). Use the *init* signal and the *frame_size* signal as shown in fig. 4 below to specify a new frame size for the component, as shown in table 3. To ensure proper operation of the device, make sure the input buffers are empty before specifying a new frame size, as the interleaver parameters are computed each time a new value is specified for the frame size. The *init* signal can also be used to perform a device “soft” reset by asserting *init* without changing the *frame_size*.

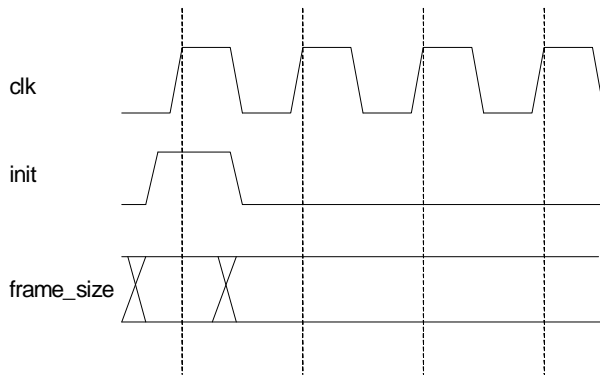


Figure 3: Initialization Timing

In order to decode using both normal and interleaved data, an entire frame must be loaded into the input buffer before the decoding process will start. The decoding will start when the *start_decode* signal is asserted.

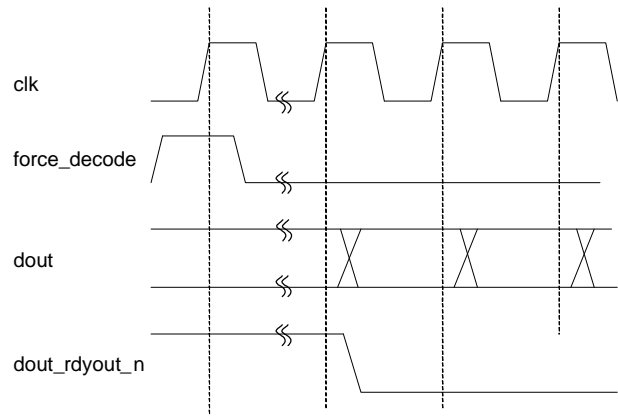


Figure 4: Start Decode Operation

Input Flow Control

The input flow control signals consist of *din_rdyin_n* and *din_rdyout_n*. These signals accompany the data in signal *din*. A ‘0’ on the *din_rdyin_n* indicates to the device that valid data is being shifted into the device on *din*. The device uses *din_rdyout_n* to indicate that it’s able to accept more data. Proper input operation is simple: valid data is flowing into the device’s input buffers when both *din_rdyin_n* and *din_rdyout_n* are logic ‘0’. Because there is an input “pre-buffering” circuit that allows zero-wait-state input operation, the *din_rdyout_n* signal can effectively be ignored in the middle of loading a frame into the device.

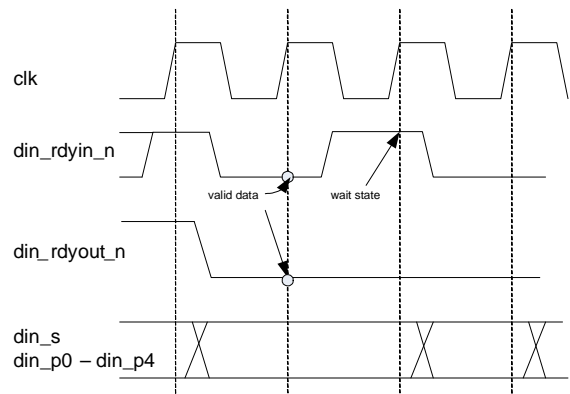


Figure 5: Input Flow Control

Output Flow Control

The output flow control signals consist of *dout_rdyin_n* and *dout_rdyout_n*. These signals accompany the data signals on *dout* out of the device. A '0' on the *dout_rdyin_n* indicates to the device that it's OK to shift data out of the device. The device uses *dout_rdyout_n* to indicate that it has valid data to send. Proper output operation is simple: valid data is flowing out of the device when both *dout_rdyin_n* and *dout_rdyout_n* are logic '0'. The *dout_rdyin_n* signal can be tied low for fastest operation.

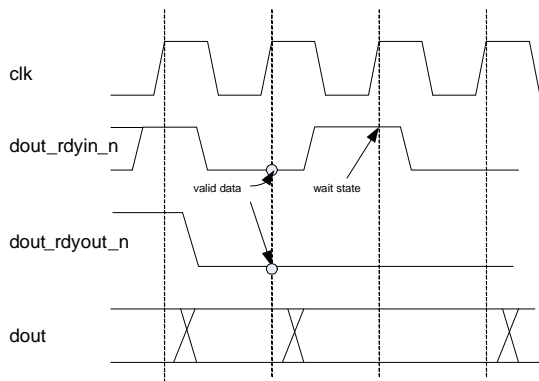


Figure 6: Output Flow Control

Module Verification

The SAL50101D has been subjected to extensive verification to ensure the highest quality product possible. A comprehensive test plan was implemented which included the following:

- All WiMAX defined block sizes
- High-quality random data source
- High-quality random noise source
- Extensive flow-control simulations
- Extensive verification and analysis of device control parameters dev_const and max_extr.
- Verification of operation against known data sequences

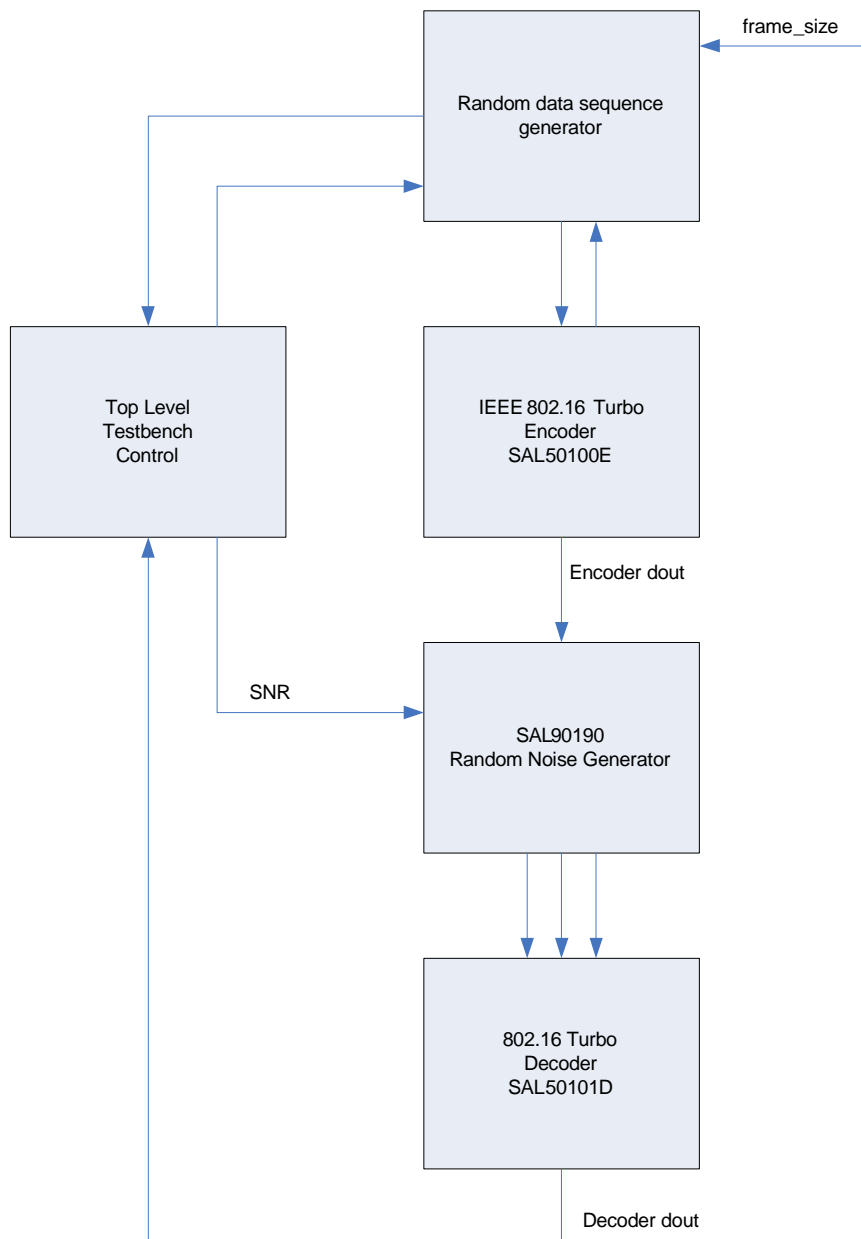
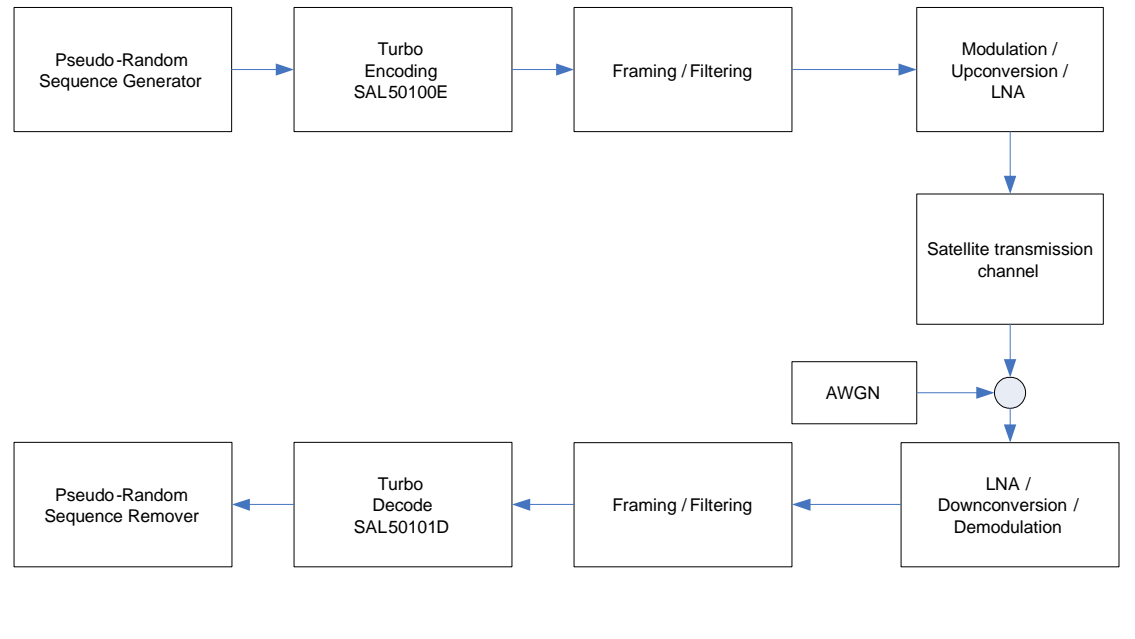


Figure 8: Testbench Block Diagram

Application: Wireless Internet System

Parallel Concatenated Convolutional Codes (PCCC) offer the best error correction performance of any known codes for code rates < 0.7 and moderate frame sizes (~ 1024 bits). The SAL50101D is designed specifically for use in wireless WAN systems.



Ordering Information

Salamander Error Correction currently has 3 WiMAX-compatible turbo decoder IP modules available:

SAL50100D Low Power

SAL50101D Standard Version

SAL50102D High Performance

About Salamander:

Salamander Error Correction develops and sells error correction modules of the highest quality worldwide.

Salamander Error Correction is a division of Komodo Industries, Inc.

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