



Features

- CCSDS 131.0-B-1 compatible
- Constraint length 7
- Nominal code rate 1/2
- Punctured rates 2/3, 3/4, 5/6, 7/8
- Simple handshake protocol for reliable interfacing
- Fully synchronous design
- Very high speed operation
- Comprehensive verification plan provided

General Description

The SAL40300E consists of verilog IP for implementing the CCSDS compatible convolutional encoder. The basic code is a rate 1/2 constraint length 7 transparent code which is well suited to channels with predominantly Gaussian noise. The device supports the nominal rate 1/2 code as well as all the punctured rates as defined in the spec.

The encoder is of the non-systematic non-recursive type, with connection polynomials $g_1 = 171$ and $g_2 = 133$. The output of g_2 is inverted in the non-punctured (rate 1/2) mode.

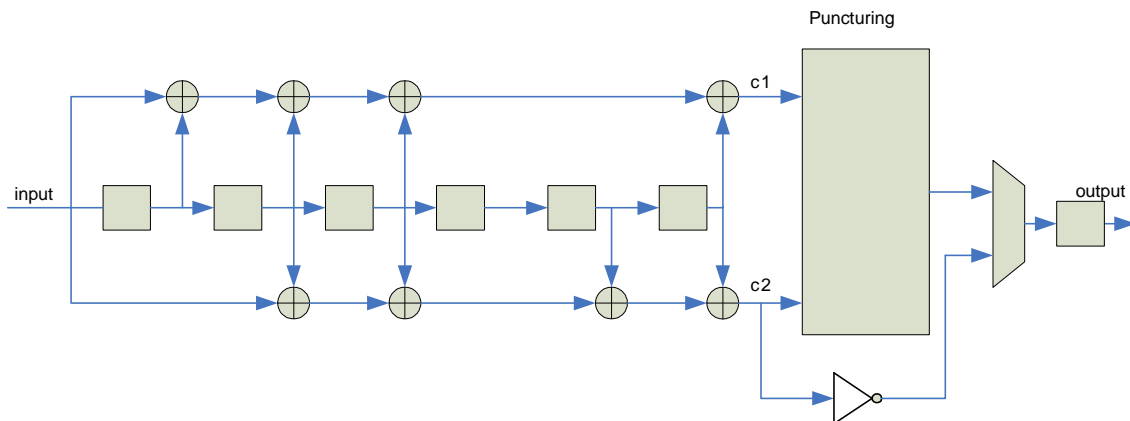


Figure 1: Encoder Block Diagram

Theory of Operation

The SAL40300E is a CCSDS-compatible (7,1/2) convolutional encoder. Its operation is very simple: a serial stream of data is shifted into the device, and an encoded serial data stream is shifted out of the device. Refer to figure 1. If the **punct** bit is not set, then puncturing is not enabled and the code is a rate 1/2 code, i.e., 2 bits are shifted out of the encoder for every bit shifted into the encoder. The bits are output in the order c1(1), c2(1)/, c1(2), c2(2)/, etc., where the slash indicates that the c2 bits are inverted. The c2 bits are inverted to ensure that there are sufficient bit transitions in the output of the encoder to allow the receiver to achieve bit synchronization.

Punctured output

If the **punct** bit is set, then some of the bits are removed from the nominal rate 1/2 output by a technique known as puncturing to achieve a higher code rate. Available code rates are 2/3, 3/4, 5/6, and 7/8. Although these rates make more efficient use of the available channel bandwidth, they suffer in their error correcting performance due to the removal of some redundant bits in the output. The puncture patterns are shown below:

Because the inverter is not used with the punctured codes, the CCSDS recommendations provide an optional randomizer for the outgoing bit stream, if the user can't ensure sufficient bit transitions by other means.

Puncture pattern 1 = transmit 0 = don't transmit	Code Rate	Output Sequence
C1: 1 0 C2: 1 1	2/3	c1(1), c2(1), c2(2), ...
C1: 1 0 1 C2: 1 1 0	3/4	c1(1), c2(1), c2(2), c1(3), ...
C1: 1 0 1 0 1 C2: 1 1 0 1 0	5/6	c1(1), c2(1), c2(2), c1(3), c2(4), c1(5), ...
C1: 1 0 0 0 1 0 1 C2: 1 1 1 1 0 1 0	7/8	c1(1), c2(1), c2(2), c2(3), c2(4), c1(5), c2(6), c1(7), ...

Table 1. Puncture patterns

Signal Descriptions

The module pinout is shown in the figure below, and in table 1. The signals are conveniently organized into functional groups as follows:

Clock and Reset

The design is fully synchronous with a single clock signal. The reset signal is synchronous and needs to be asserted for at least one full clock cycle to reset internal logic.

Control signals

Two signals control flow of data into the device, *din_rdyin_n* and *din_rdyout_n*. The *din_rdyin_n* signal indicates that data into the device is valid. The *din_rdyout_n* signal indicates that the device is ready to receive data.

Two signals control flow of data out of the device, *dout_rdyout_n* and *dout_rdyin_n*. The *dout_rdyout_n* signal indicates that data out of the device is valid. The *dout_rdyin_n* signal indicates to the device that it's OK to shift data out of the device.

Data signals

The data are clocked in on *din* and clocked out on *dout*.

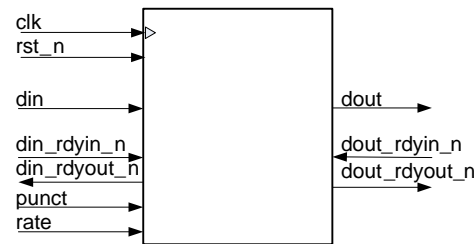


Figure 2: Component pinout

Pin	Sense	Width	Description
clk	in	1	Clock
rst_n	in	1	Synchronous reset
punct	in	1	When set, code is punctured
rate	in	2	Code rate: 00 = 2/3, 01 = 3/4, 10 = 5/6, 11 = 7/8
din	in	1	Serial data (message) in
din_rdyin_n	in	1	Indicates serial data in is valid
din_rdyout_n	out	1	'1' indicates data in, '0' = ignore input (during parity phase)
dout	out	8	Data out
dout_rdyin_n	out	1	When '1', indicates data out, else it's parity
dout_rdyout_n	out	1	Indicates that data is available to be shifted out

Table 2. Component pinout

Waveforms

Input

The input functional timing is shown below. *Din_rdyin_n* is used as an input data enable, *din_rdyout_n* is used to indicate when the device is ready to receive data.

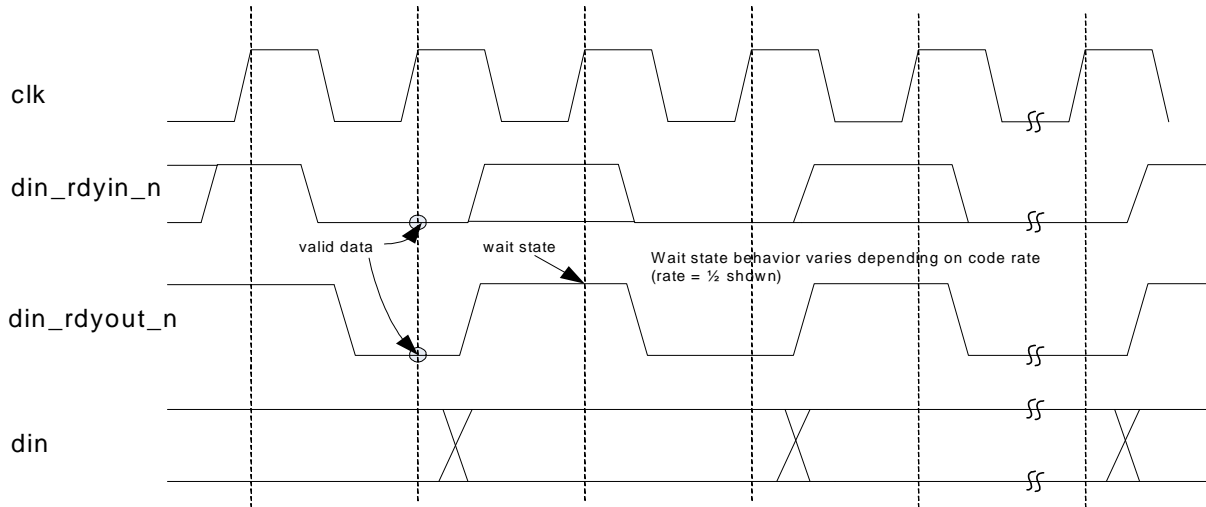


Figure 3: Input timing

Output

The output functional timing is shown below. *Dout_rdyout_n* is used as an output data ready indication, *dout_rdyin_n* is used to indicate to the device that it's OK to shift data out.

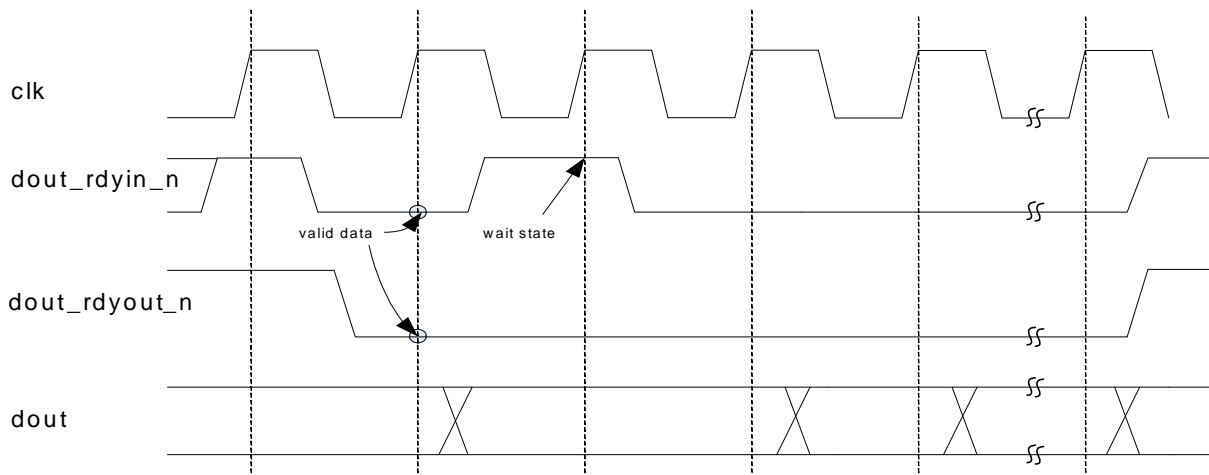


Figure 4. Output timing

Module Verification

The SAL40300E has been subjected to extensive verification to ensure the highest quality product possible. A comprehensive test plan was implemented which included the following:

- High-quality random data source
- High-quality random noise source
- Extensive flow-control simulations
- Verification of operation against known data sequences

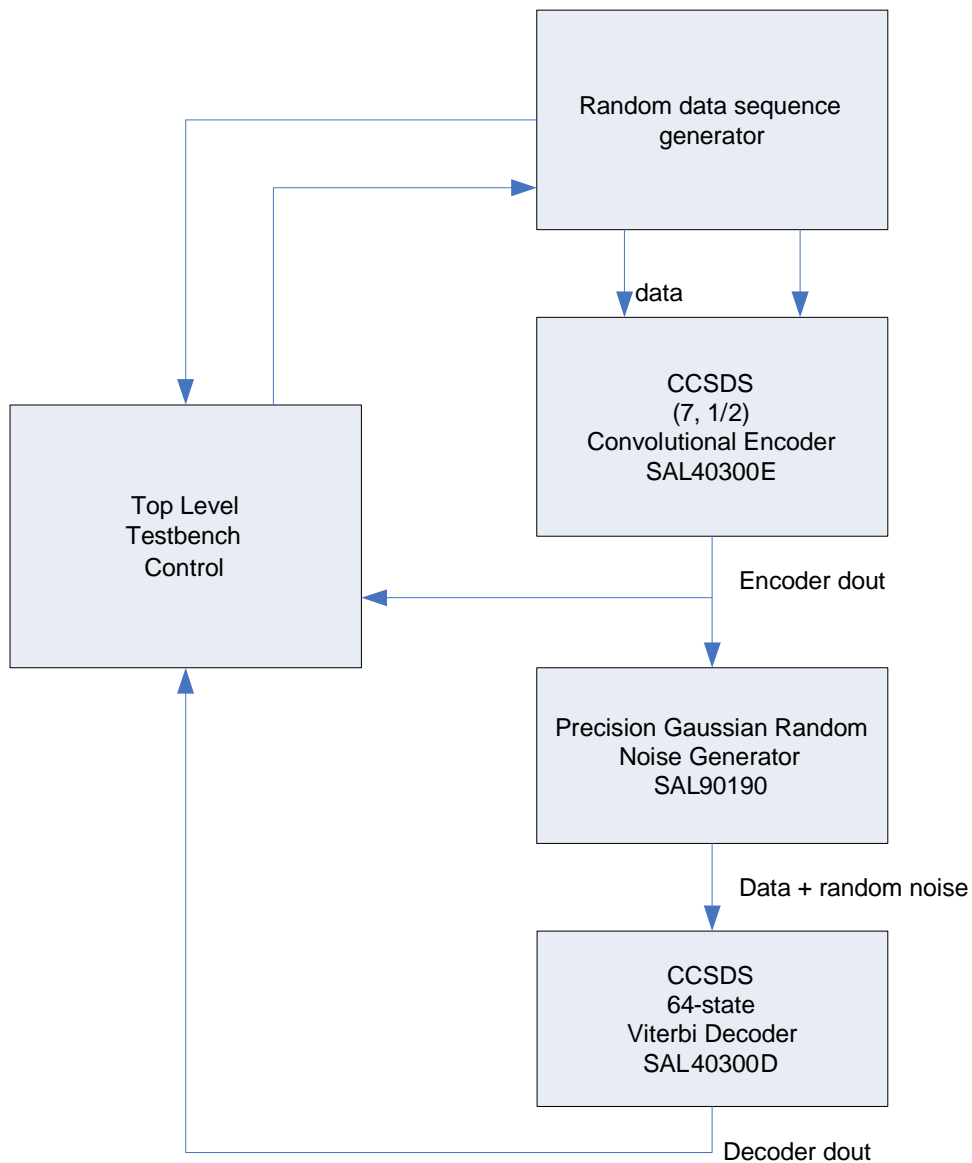
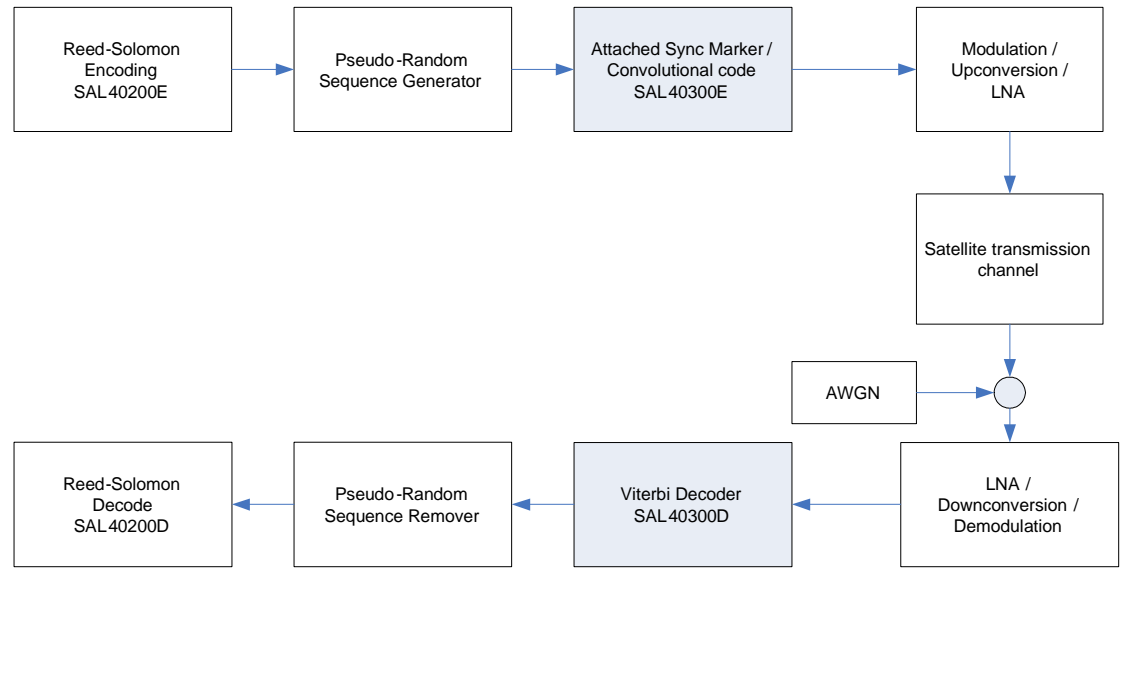


Figure 5: Testbench Block Diagram

Application: Satellite System

The CCSDS convolutional code forms an integral part of many satellite telemetry systems.



Ordering Information

Salamander Error Correction currently has 1 CCSDS-compatible convolutional encoder IP module available:

SAL40300E CCSDS convolutional encoder

About Salamander:

Salamander Error Correction develops and sells error correction modules of the highest quality worldwide.

Salamander Error Correction is a division of Komodo Industries, Inc.

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