

### Features

- For use in 3GPP (UMTS, WCDMA) systems. Fully compliant with the 3GPP standard ETSI 25.212 V4.5.0
- Double Buffered input enables high speed operation
- Generic memory interface for easy ASIC integration
- Simple handshake protocol for reliable interfacing
- Fully synchronous design
- Full 3GPP compliant hardware interleaver. No external calculation required.
- Interleaver frame size selectable on a frame-by-frame basis
- Buffer-ready interrupt provided
- Comprehensive verification plan provided
- Full block size range of 40 – 5114 bits supported

### General Description

The SAL20101D consists of verilog IP for decoding the parallel concatenated convolutional (turbo) code defined by the 3GPP standard. Refer to Fig. 1 below.

The decoder takes in 6-bit values for the unencoded (“systematic”) data and two parity values, one which is the result of encoding the data with a simple convolutional encoder and one which is the result of encoding a permuted version of the data through an identical simple convolutional encoder. The permutation is described in detail in the 3GPP specification.

The data are operated on iteratively by the Maximum A Posteriori (MAP) decoder module, first looking at the normal ordered data and parity, then looking at the interleaved sequence and parity. At each step in the process a correction factor is refined and stored as “extrinsic” data for use in the following step.

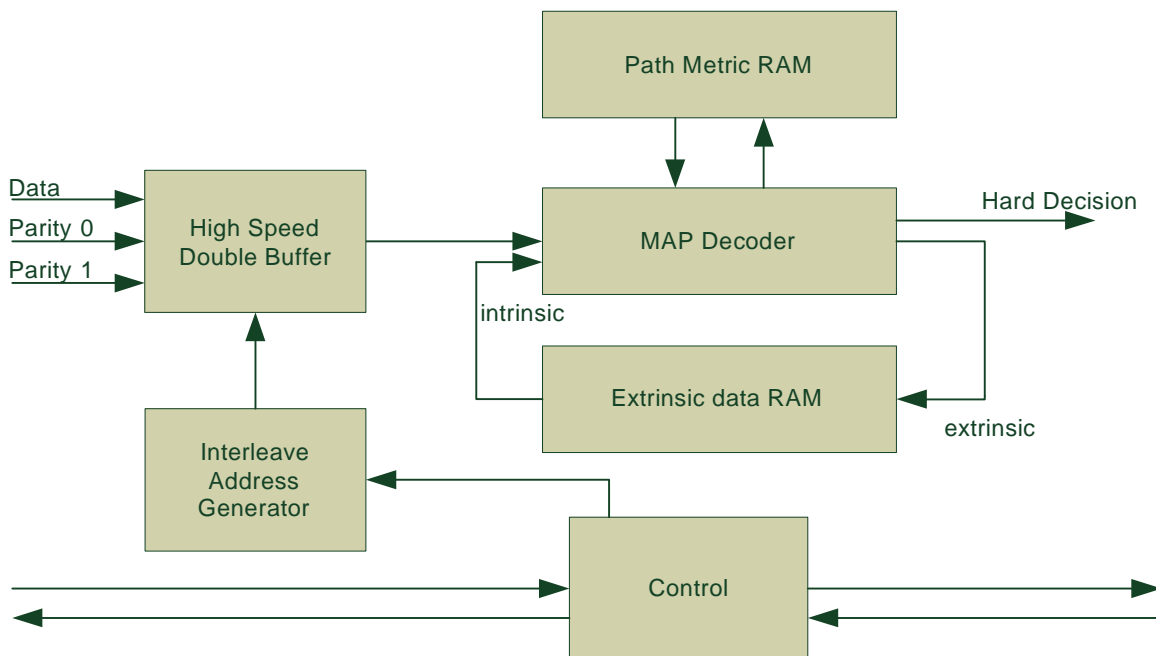


Figure 1: Decoder Block Diagram

## Theory of Operation

The SAL20101D is a self-contained, high quality error correction coder designed specifically for use in UMTS systems. The emphasis for the –20101D product is on achieving superior error correction performance at a moderate complexity. The reader is referred to the SAL20100D product for out lowest power and most efficient device. For the highest bitrate performance (at the expense of higher complexity) the reader is referred to the SAL20102D product.

The device receives 6-bit 2's-compliment data for unencoded data, parity, and interleaved parity. Data can also be received as signed-magnitude or unsigned binary, based on the *input\_mode* signal.

input_mode[1:0]	Definition
00	6-bit 2's compliment
01	6-bit signed magnitude
10	6-bit unsigned binary
11	6-bit 2's compliment

Table 1. input\_mode

The heart of the decoder is a soft-in / soft-out (SISO) decoder module that performs the full log-MAP algorithm iteratively.

### The Decoder Constant

Because the decoder core operates in the logarithmic domain, the input data need to be converted to a logarithmic (log likelihood ratio) form. This reduces to multiplication of the input data by a constant based on the estimated signal to noise ratio of the channel.

The value of the decoder constant is calculated using the formula:

$$C = A\sigma^2\sqrt{m}/2 \quad (1)$$

Where  $\sigma^2$  is the normalized noise variance. It has been shown [2] that no noise estimation is better than poor noise estimation, so the input scaling can optionally be disabled.

### Max Extrinsic

In addition to input scaling, the extrinsic correction term can be limited to limit the rate at which the decoder converges on a solution.

### Num Iterations

The number of decoder iterations can be specified using the *num\_its* signal. The default value is 4.5. Optionally the device can be allowed to perform early termination, if the decoder converges on a solution before the specified number of iterations.

### Mode Bits

There are a number of mode bits beside the input and output mode bits, and they are shown in the table below.

mode[4:0]	Definition, if set
mode[0]	Use decoder_const
mode[1]	Use max_extr
mode[2]	Use num_its, else use 4.5 iterations
mode[3]	Use early termination, if possible
mode[4]	Use force_decode (see below)

Table 2. mode bits

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## Output Mode

Data output can be either serial or parallel, depending on the value of the **out\_mode** signal.

out_mode	Definition, if set
out_mode	Data out is 32-bit parallel

Table 3. output mode

If the **out\_mode** bit is not set, the data appear one bit at a time on **dout[0]**. If the bit is set, the data come out 32 bits at a time on **dout[31:0]**.

## Device Operation

If the “Use force\_decode” option (mode[4]) is set, decoding begins when the **force\_decode** signal is asserted, otherwise decoding will begin automatically when a frame’s worth of data (plus 12 tail bits) has been loaded into the device. In devices with double-buffered input the device will accept a second buffer while processing the first.

## Signal Descriptions

The module pinout is shown in the figure below, and in table 1. The signals are conveniently organized into functional groups as follows:

### Clock and Reset

The design is fully synchronous with a single clock signal. The reset signal is synchronous and needs to be asserted for at least one full clock cycle to reset internal logic.

### Control signals

Init, frame\_size, d\_const, max\_extr, in\_mode and out\_mode are control signals whose operation is described below.

### Data signals

The din\_s, din\_p, din\_p\_prime are 6-bit input signals representing the systematic data and the two parity signals defined in the spec. Dout is the serial or parallel output decoded data.

The data input to the device are stored internally in FIFO order, the first bit being bit 0 of the data frame. In addition to the data frame, the device expects to see 12 trellis termination or “tail” bits as defined in the spec.

The data out of the device are in FIFO order, and therefore don't require an address to access them. The data can either be read out in serial fashion on bit 0 of dout, or in parallel fashion, depending on the value of out\_mode.

### Flow control signals

The “rdy\_in\_n” signals are active low indicators to the device that data is available on the input or that the external logic is able to accept data.

The “rdyout\_n” signals are active low indicators from the device that it is ready to accept data on the input or to shift out data on the output

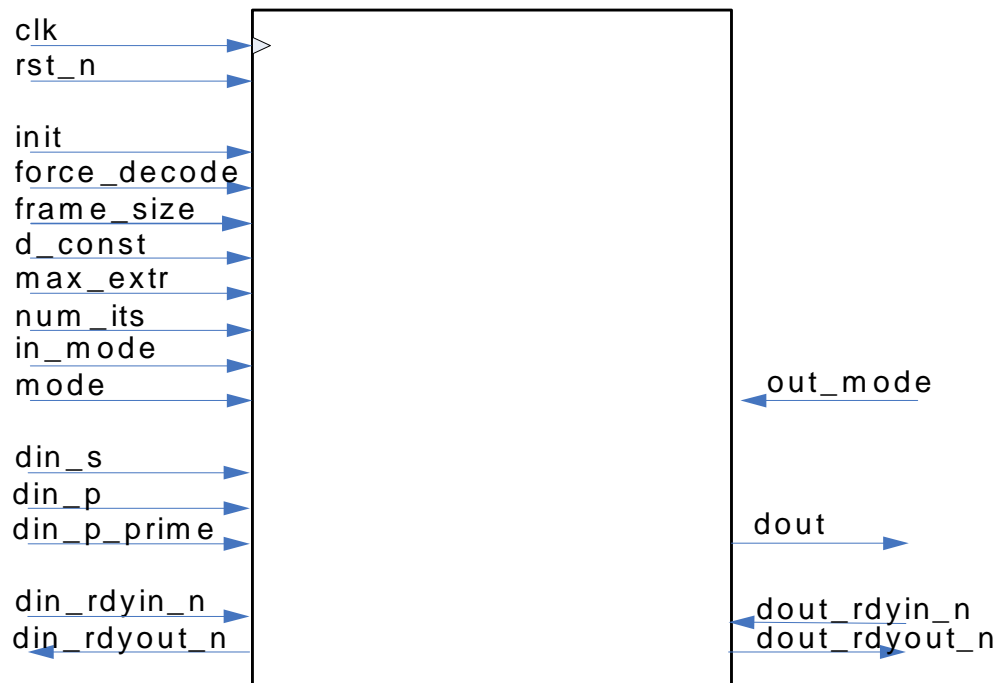


Figure 2: Component Pinout

Pin	Sense	Width	Description
clk	in	1	clock
rst_n	in	1	synchronous reset
din_s	in	6	serial data (message) in
din_p	in	6	serial parity data in
din_p_prime	in	6	serial interleaved parity data in
din_rdyin_n	in	1	indicates serial data in is valid
din_rdyout_n	out	1	indicates module ready to accept data (not all input buffers full)
dout	out	32	decoded data out (serial or parallel depending on mode)
dout_rdyin_n	in	1	indicates to the module that it's ok to shift data out
dout_rdyout_n	out	1	indicates that data is available to be shifted out
init	in	1	initializes the interleaver and loads the block size
force_decode	in	1	when enabled, decoding begins when this signal is asserted
frame_size	in	13	indicates size of current block. Initialized with "init" signal.
dec_const	in	8	decoder constant, based on estimated noise (see description above)
max_extr	in	8	maximum allowable extrinsic data (see description above)
in_mode	in	2	input mode: specify the data format of input bits
mode	in	5	various mode affecting device operation
out_mode	in	1	specify serial or parallel output format
Table 4. Pin Definitions			

## Waveforms

### Initialization

The frame size defaults to 40 bits (the minimum number specified in the 3GPP spec). Use the *init* signal and the *frame\_size* signal as shown in fig. 4 below to specify a new frame size (in bits) for the component. To ensure proper operation of the device, make sure the input buffers are empty before specifying a new frame size, as the interleaver parameters are computed each time a new value is specified for the frame size. Thus the *init* signal can also be used to perform a device “soft” reset by asserting *init* without changing the *frame\_size*.

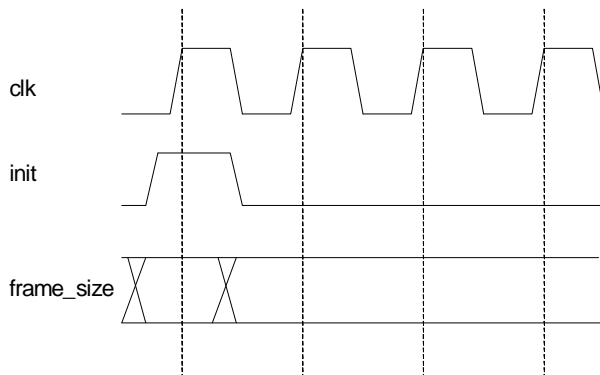


Figure 3: Initialization Timing

In order to decode using both normal and interleaved data, an entire frame must be loaded into the input buffer before the decoding process will start. The decoding will start automatically when the correct number of bits are shifted into the component. Alternatively, the *force\_decode* signal can be used to force the decoder to begin decoding the data.

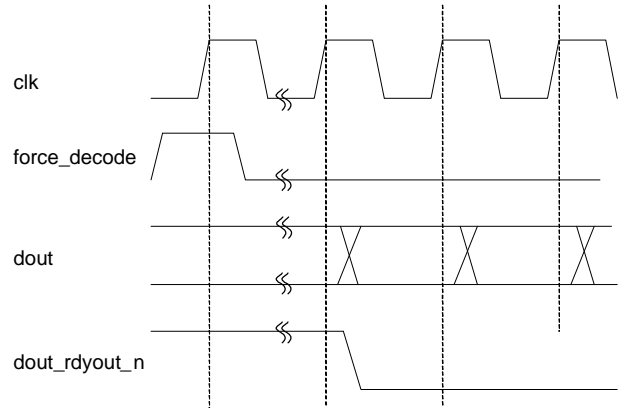


Figure 4: Force Decode Operation

### Input Flow Control

The input flow control signals consist of *din\_rdyin\_n* and *din\_rdyout\_n*. These signals accompany the data in signal *din*. A ‘0’ on the *din\_rdyin\_n* indicates to the device that valid data is being shifted into the device on *din*. The device uses *din\_rdyout\_n* to indicate that it’s able to accept more data. Proper input operation is simple: valid data is flowing into the device’s input buffers when both *din\_rdyin\_n* and *din\_rdyout\_n* are logic ‘0’. Because there is an input “pre-buffering” circuit that allows zero-wait-state input operation, the *din\_rdyout\_n* signal can effectively be ignored in the middle of loading a frame into the device.

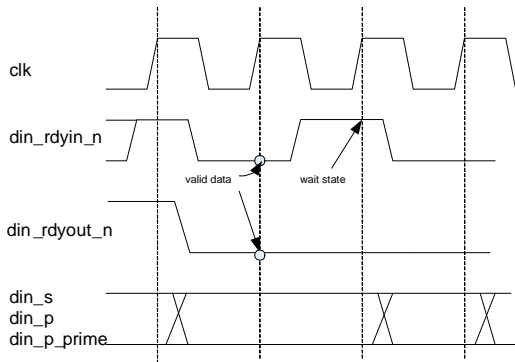


Figure 5: Input Flow Control

### Output Flow Control

The output flow control signals consist of **dout\_rdyin\_n** and **dout\_rdyout\_n**. These signals accompany the data signals on **dout** out of the device. A '0' on the **dout\_rdyin\_n** indicates to the device that it's OK to shift data out of the device. The device uses **dout\_rdyout\_n** to indicate that it has valid data to send. Proper output operation is simple: valid data is flowing out of the device when both **dout\_rdyin\_n** and **dout\_rdyout\_n** are logic '0'. The **dout\_rdyin\_n** signal can tied low for fastest operation.

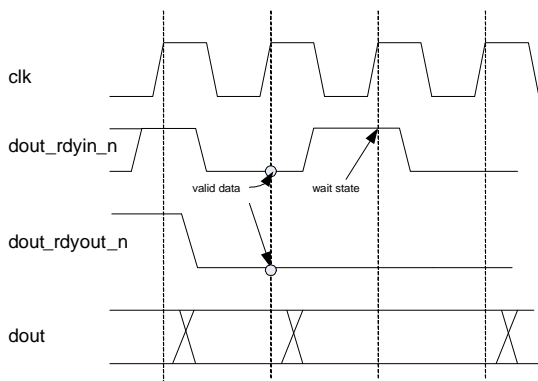


Figure 6: Output Flow Control

### Tail Bits

In addition to the data frame message bits, there are 12 bits called tail bits that are sent by the turbo encoder. This is because the encoding process is completed by forcing the constituent coders to a known state (the 000 state, in this case). After the data frame has been sent, the first constituent coder is clocked three times while the second constituent coder is disabled, then the second constituent coder is clocked three times, resulting in a total of twelve tail bits:  $X_{k+1}, Z_{k+1}, X_{k+2}, Z_{k+2}, X_{k+3}, Z_{k+3}, X'_{k+1}, Z'_{k+1}, X'_{k+2}, Z'_{k+2}, X'_{k+3}, Z'_{k+3}$ .

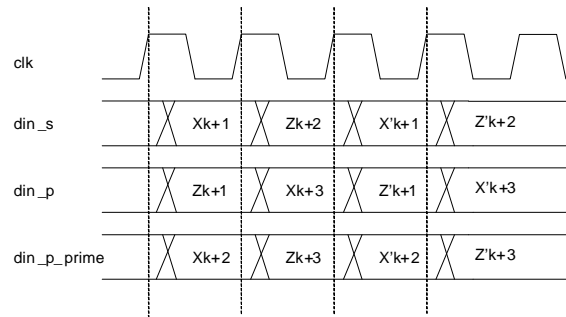


Figure 7: Tail Bits

These tail bits are received as shown in the figure, and the decoder will use the information to establish the correct starting point when working backward through the code trellis.

## Module Verification

The SAL20101D has been subjected to extensive verification to ensure the highest quality product possible. A comprehensive test plan was implemented which included the following:

- All 3GPP frame sizes from 40 to 5114 bits
- High-quality random data source
- High-quality random noise source
- Extensive flow-control simulations
- Extensive verification and analysis of device control parameters dev\_const and max\_extr.
- Verification of operation against known data sequences

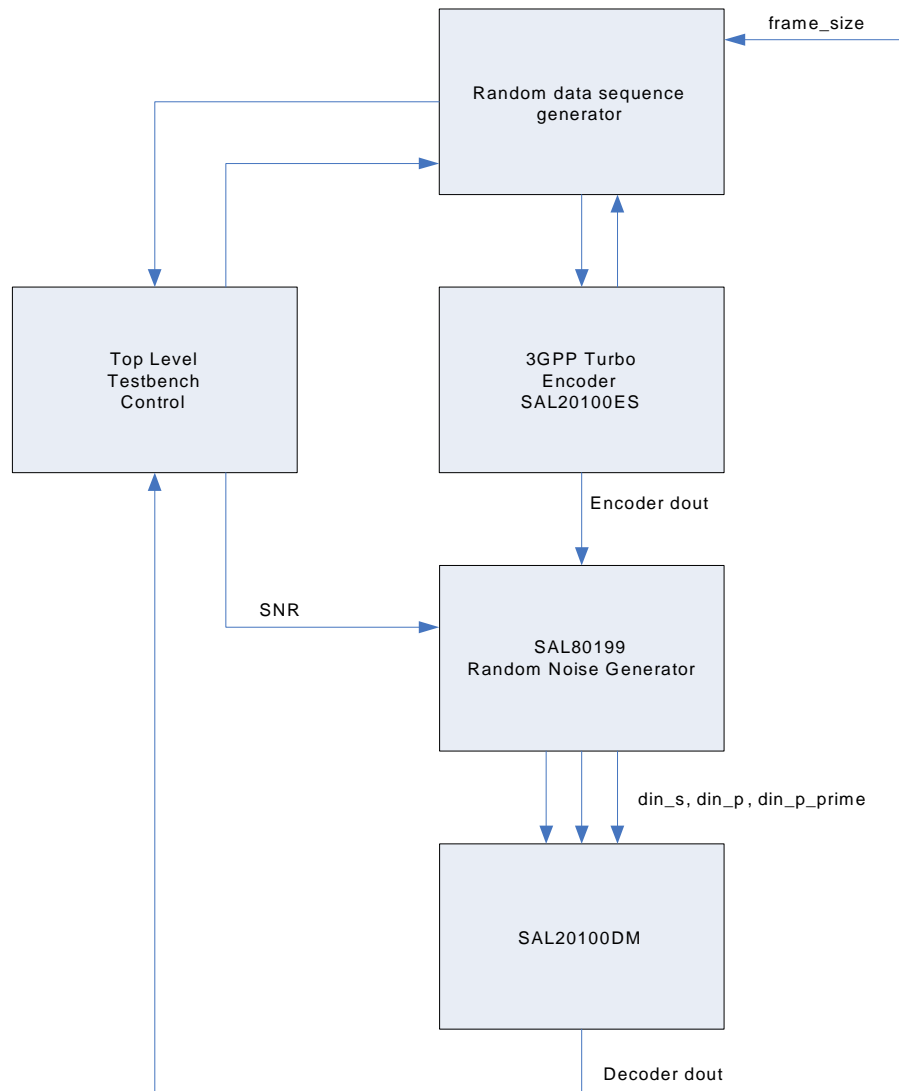
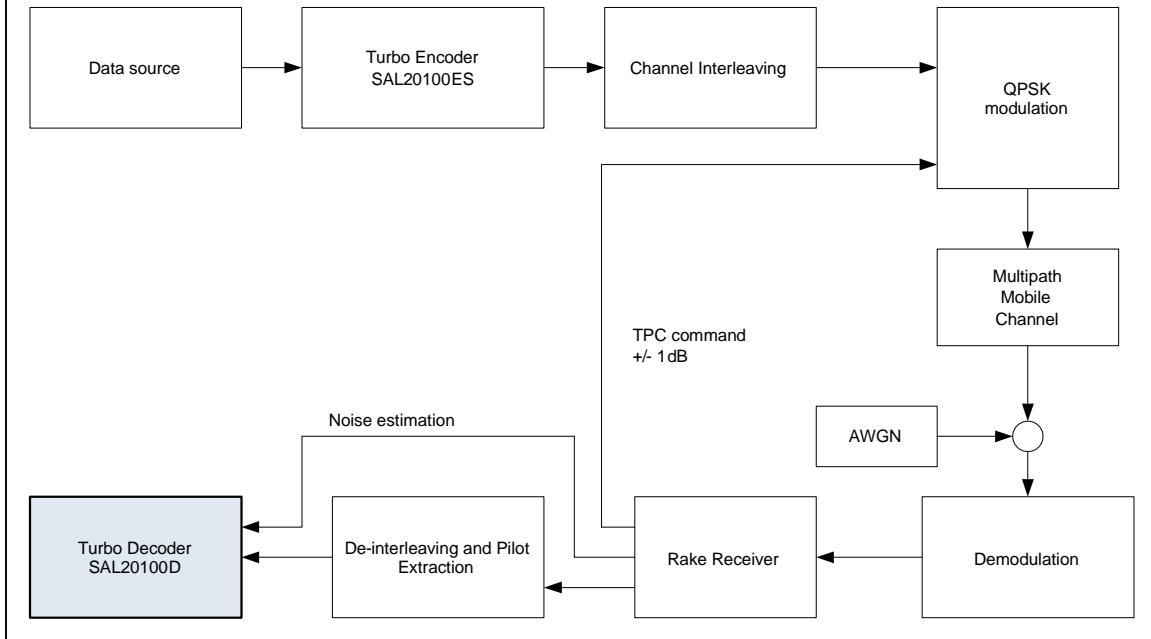


Figure 8: Testbench Block Diagram

## Application: UMTS

Parallel Concatenated Convolutional Codes (PCCC) offer the best error correction performance of any known codes for code rates  $< 0.7$  and moderate frame sizes ( $\sim 1024$  bits). The SAL20101D is designed specifically for use in UMTS systems.



## Ordering Information

Salamander Error Correction currently has 3 3GPP-compatible turbo decoder IP modules available:

**SAL20100D** Low Power

**SAL20101D** Standard Version

**SAL20102D** High Performance

## About Salamander:

**Salamander Error Correction** develops and sells error correction modules of the highest quality worldwide.

Salamander Error Correction is a division of Komodo Industries.

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