



Features

- Flexible, Generic Viterbi decoder
- Constraint lengths 5, 7, and 9
- Programmable polynomial
- Variable frame size: 32-4096 bits
- Three code rates 1/2, 1/3, 1/4
- Simple handshake protocol for reliable interfacing
- Fully synchronous design
- High speed operation > 32 MHz
- Erasure support
- 5-bit soft input
- 16 clocks-per-bit operation
- Comprehensive verification plan provided

General Description

The SAL10300D consists of verilog IP for implementing a generic 16, 64, or 256-state Viterbi decoder. The basic code is a constraint length 5, 7, or 9 transparent code which is well suited to channels with predominantly Gaussian noise.

The decoder uses the maximum-likelihood (Viterbi) algorithm to decode a generic convolutional code. The code is of the non-systematic non-recursive type. Connection polynomials can be specified for rate 1/2, rate 1/3, and rate 1/4 convolutional codes.

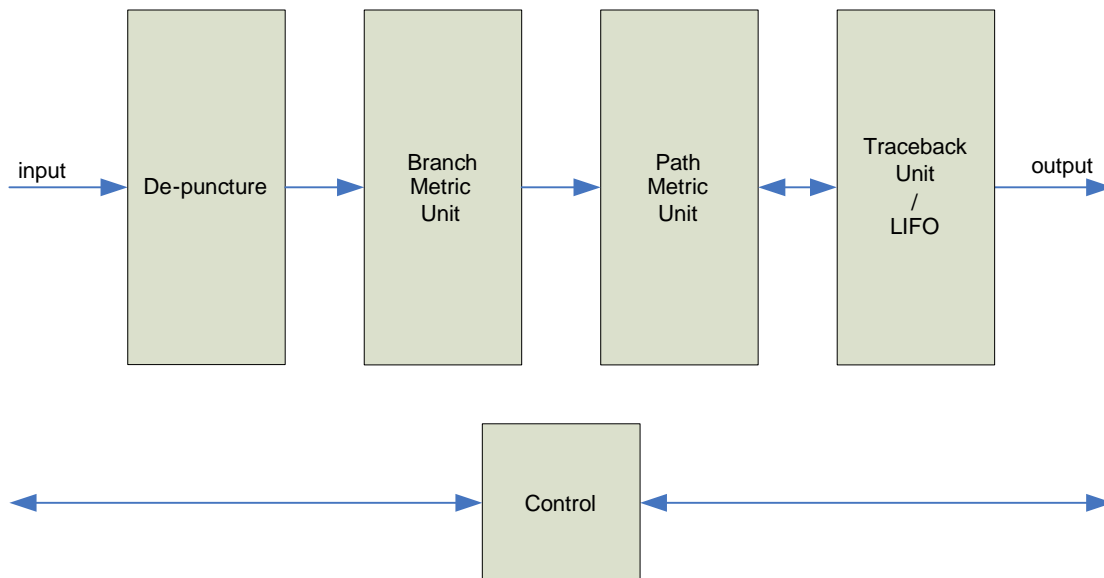


Figure 1: Decoder Block Diagram

Theory of Operation

The SAL10300D is a generic 16, 64, or 256-state Viterbi decoder. The device accepts 5-bit soft input data samples formatted as shown in table 1.

The branch metric unit assigns to the incoming data a set of metrics based on different assumptions of the current state of the code trellis. The branch metrics are then passed to the path metric unit and are added to the accumulated path metric and the most likely path metric is selected and stored for subsequent comparison.

After a traceback depth's worth of data is captured, the traceback unit works backward through the trellis, pulling the most likely bits from the survivor memory as it goes. The data are stored in a Last-In-First-Out (LIFO) buffer and made available to the output of the device at the end of the traceback sequence.

in_mode[1:0]	Input format
00	2's compliment
01	sign-magnitude
10	binary
11	hard input

Table 1. input mode

Signal Descriptions

The module pinout is shown in the figure below, and in table 1. The signals are conveniently organized into functional groups as follows:

Clock and Reset

The design is fully synchronous with a single clock signal. The reset signal is synchronous and needs to be asserted for at least one full clock cycle to reset internal logic.

The init signal is used as a “soft” reset signal, to return the device to the zero state of the trellis.

Control signals

Two signals control flow of data into the device, *din_rdyin_n* and *din_rdyout_n*. The *din_rdyin_n* signal indicates that data into the device is valid. The *din_rdyout_n* signal indicates that the device is ready to receive data.

Two signals control flow of data out of the device, *dout_rdyout_n* and *dout_rdyin_n*. The *dout_rdyout_n* signal indicates that data out of the device is valid. The *dout_rdyin_n* signal indicates to the device that it’s OK to shift data out of the device.

Sync

The sync signal is used when the bit synchronization is not known. Asserting this signal causes the device to make multiple attempts to decode the data based on initial state assumptions and to adjust those assumptions based on the relative values of the path metrics. This signal should not be used in normal operation when the frame sync is known, because its use affects the throughput and power consumption of the device.

Data signals

The data are clocked in on *din* and clocked out on *dout*.

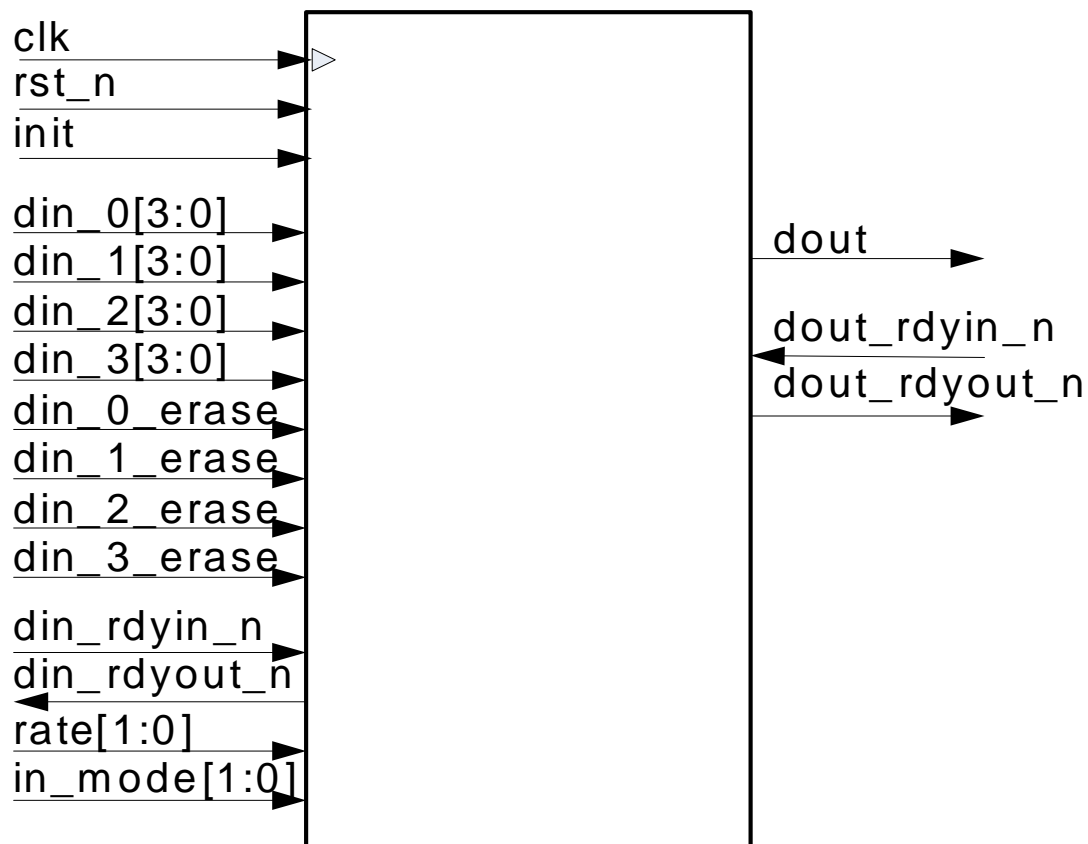


Figure 2: Component pinout

Pin	Sense	Width	Description
clk	in	1	Clock
rst_n	in	1	Synchronous reset
init	in	1	Soft reset. Sets the trellis state to the zero state.
rate	in	2	Code rate: 00 = 1/2, 01 = 1/3, 10 = 1/4, 11 = 1/4
in_mode	in	2	Input data format (see table 1)
din_0	in	4	Serial data (message) in
din_1	in	4	Serial data (message) in
din_2	in	4	Serial data (message) in
din_3	in	4	Serial data (message) in
din_0_erase	in	1	When asserted, indicates an erasure on din_0
din_1_erase	in	1	When asserted, indicates an erasure on din_1
din_2_erase	in	1	When asserted, indicates an erasure on din_2
din_3_erase	in	1	When asserted, indicates an erasure on din_3
din_rdyin_n	in	1	Indicates serial data in is valid
din_rdyout_n	out	1	Indicates that the device is ready to accept data in
dout	out	1	Data out
dout_rdyin_n	in	1	Indicates to the device that it's ok to shift data out
dout_rdyout_n	out	1	Indicates that data is available to be shifted out
Table 3. Component pinout			

Waveforms

Input

The input functional timing is shown below. *Din_rdyin_n* is used as an input data enable, *din_rdyout_n* is used to indicate when the device is ready to receive data.

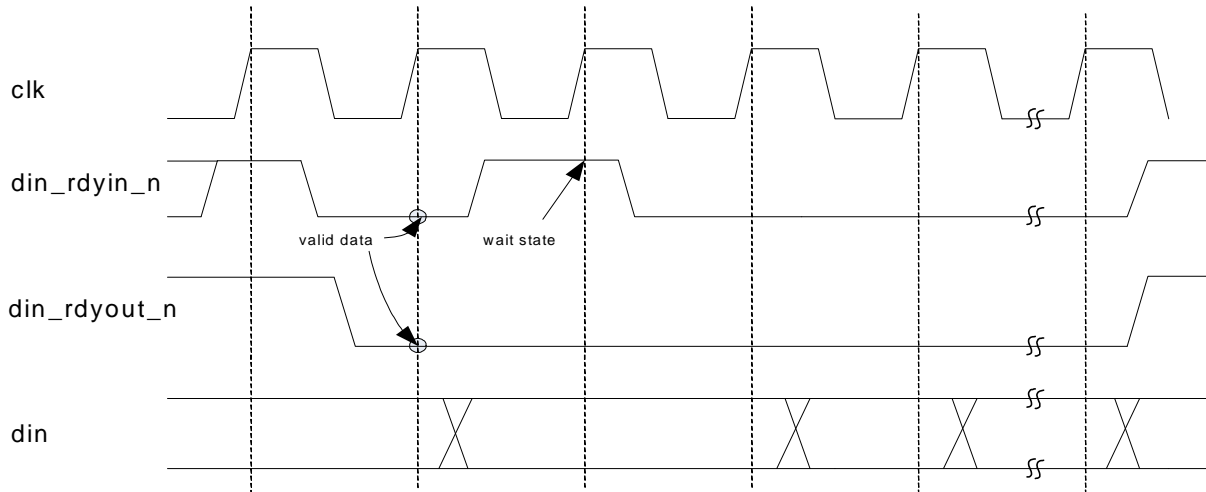


Figure 3: Input timing

Output

The output functional timing is shown below. *Dout_rdyout_n* is used as an output data ready indication, *dout_rdyin_n* is used to indicate to the device that it's OK to shift data out.

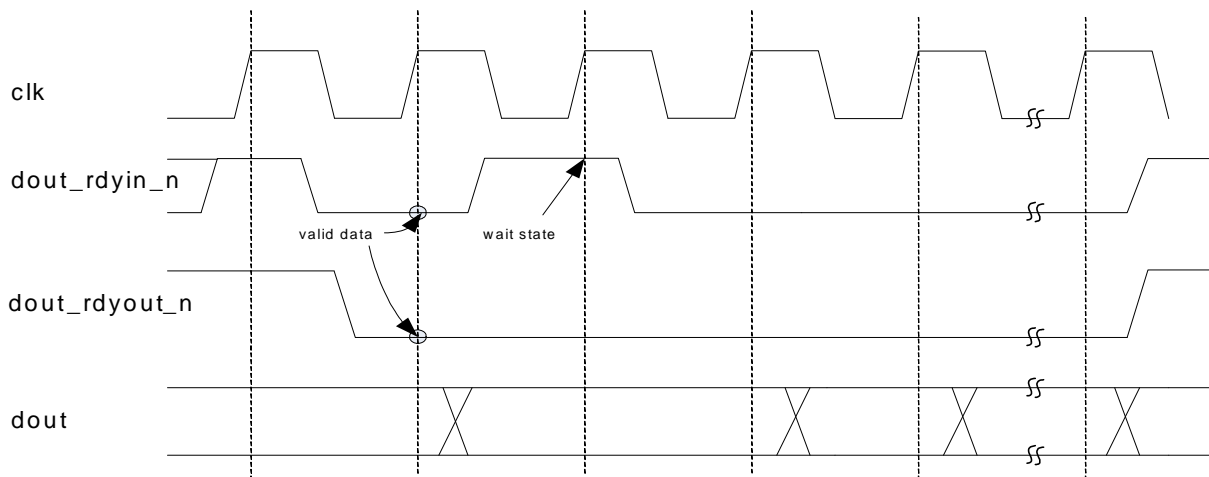


Figure 4. Output timing

Module Verification

The SAL10300D has been subjected to extensive verification to ensure the highest quality product possible. A comprehensive test plan was implemented which included the following:

- High-quality random data source
- High-quality random noise source
- Extensive flow-control simulations
- Verification of operation against known data sequences

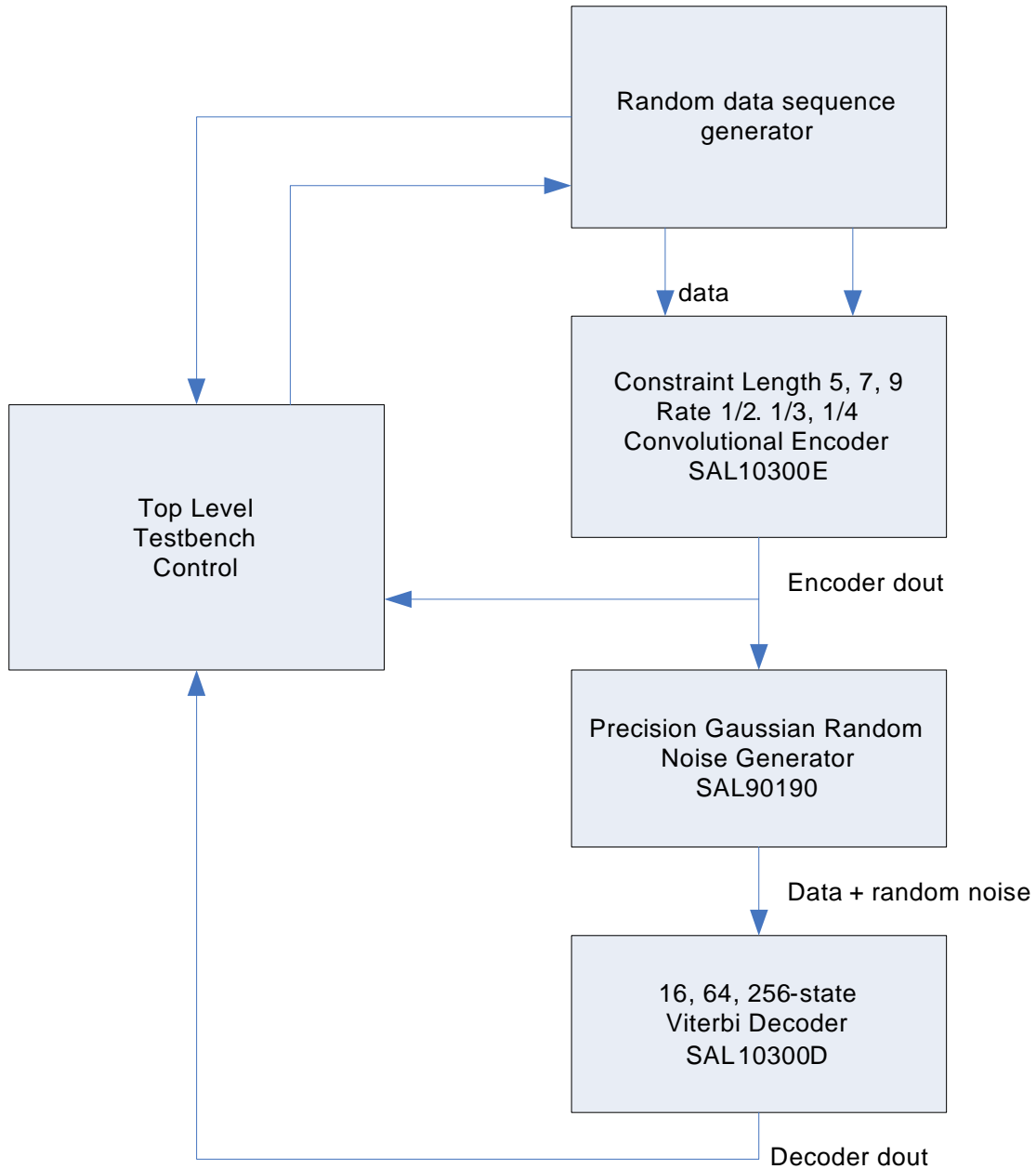
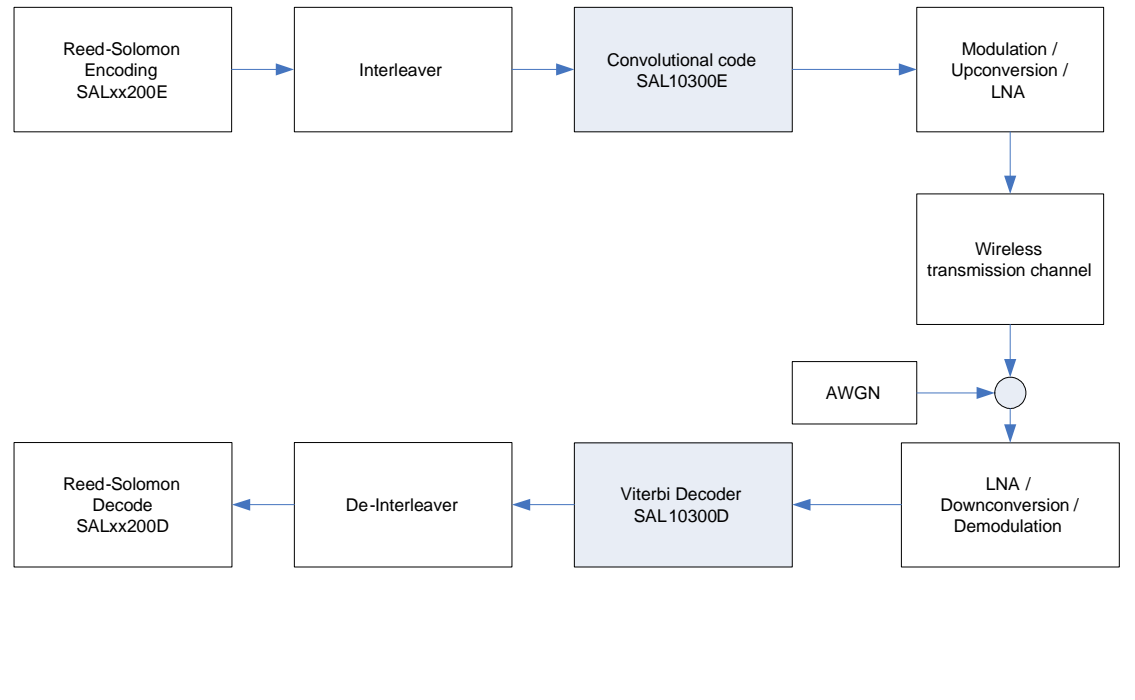


Figure 5: Testbench Block Diagram

Application: Wireless Internet System

A convolutional code forms an integral part of a wireless Internet telemetry system.



Ordering Information

Salamander Error Correction currently has 1 Flexible Viterbi decoder IP module available:

SAL10300D Viterbi decoder, medium speed

About Salamander:

Salamander Error Correction develops and sells error correction modules of the highest quality worldwide.

Salamander Error Correction is a division of Komodo Industries, Inc.

Salamander Error Correction:
5330 Carroll Canyon Rd
San Diego, CA 92121
(858) 373-2112
fax: (858) 373-1224
sales@salamander-ecc.com
www.salamander-ecc.com